|  |
| --- |
| SRM INSTITUTE OF SCIENCE AND TECHNOLOGY  Faculty of Engineering and Technology  Department of Electronics and Communication Engineering |
| **18ECC206J - VLSI Design**  **VI Semester, 2022-2023 (EVEN Semester)** |

**Title of Mini Project :**

**Date of Submission :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks Obtained** | | |
| **Name:** | **Name** | **Name** |
| **Register No.** | **Register No.** | **Register No.** |
| Design Code | 25 |  |  |  |
| Demo verification &viva | 10 |  |  |  |
| Project Report | 05 |  |  |  |
| **Total** | **40** |  |  |  |

**REPORT VERIFICATION**

**Staff Name :**

**Signature :**

**Mini Project Content**

**1.Objective**

**2.Software Detail**

**3.Abstract /Introduction**

**4.Block Diagram/Logic Diagram/Truth table/Boolean Expression(include which is relevant to your topic)**

**5. Code**

**6. Result**

**7. Conclusion**

**Neatly align the report with proper spacing and submit PDF file for each team.**